

## 支持复位的 PCA9548A 低电压 8 通道 I<sup>2</sup>C 开关

### 1 特性

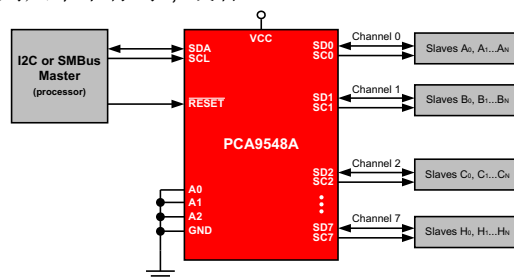
- 8 选 1 双向转换开关
- 与 I<sup>2</sup>C 总线和系统管理总线 (SMBus) 兼容
- 低电平有效复位输入
- 三个硬件地址引脚允许在 I<sup>2</sup>C 总线上使用多达八个 PCA9548A 器件
- 通过 I<sup>2</sup>C 总线实现通道选择
- 加电时所有开关通道取消选定
- 低 R<sub>ON</sub> 开关
- 支持 1.8V、2.5V、3.3V 和 5V 总线间的电压电平转换
- 加电时无干扰
- 支持热插入
- 低待机电流
- 工作电源电压范围为 2.3V 至 5.5V
- 5V 耐压输入
- 0kHz 至 400kHz 时钟频率
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 带电器件模型 (C101)

### 2 应用

- 服务器
- 路由器 (电信交换设备)
- 工厂自动化
- 具有 I<sup>2</sup>C 从地址冲突的产品 (例如, 多个完全一样的温度传感器)

### 3 说明

PCA9548A 器件配有八个可通过 I<sup>2</sup>C 总线控制的双向转换开关。SCL/SDA 上行对扩展到八个下行对, 或者



简化版原理图

通道。根据可编程控制寄存器的内容, 可选择任一单独的 SC<sub>x</sub>/SD<sub>x</sub> 通道或者通道组合。这些下游通道可用于解决 I<sup>2</sup>C 从器件地址冲突。例如, 如果应用中需要八个完全相同的数字温度传感器, 则每个通道 (0-7) 可以连接一个传感器。

发生超时或其他不当操作时, 系统主控器可通过将 RESET 输入置为低电平来复位 PCA9548A。同样, 上电复位即可取消选中所有通道并初始化 I<sup>2</sup>C/SMBus 状态机。将 RESET 置为有效也可实现复位和初始化, 并且无需将部件断电。这样可以在下游 I<sup>2</sup>C 总线卡在低电平状态时进行恢复。

由于开关上有导通栅极, 因此 VCC 引脚可用于限制将由 PCA9548A 传递的最大电压。这样就可以在每个对上使用不同的总线电压, 从而让 1.8V、2.5V 或 3.3V 部件能够在没有任何额外保护的情况下与 5V 部件通信。对于每个通道, 外部上拉电阻器将总线电压上拉至所需的电压水平。所有 I/O 引脚均可承受 5V 电压。

#### 器件信息

器件名称	封装 <sup>(1)</sup>	封装尺寸 (标称值)
PCA9548A	SSOP (24)	8.20mm × 5.30mm
	TVSOP (24)	5.00mm × 4.40mm
	SOIC (24)	15.40mm × 7.50mm
	TSSOP (24)	7.80mm × 4.40mm
	VQFN (24)	4.00mm × 4.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (April 2019) to Revision G (March 2021)	Page
• Changed the PW and RGE package values in the <i>Thermal Information</i> .	5
• Changed the V <sub>PORR</sub> row in the <i>Electrical Characteristics</i>	6
• Added V <sub>PORF</sub> row to the <i>Electrical Characteristics</i>	6
• Changed the I <sub>CC</sub> Low inputs and High inputs values in the <i>Electrical Characteristics</i>	6
• Changed the <i>Power Supply Recommendations</i>	24
Changes from Revision E (February 2015) to Revision F (April 2019)	Page
• 更新了 <a href="#">节 3</a> 部分.....	1
• Changed the <i>Pin Configuration</i> images.....	3
• Updated Pin Name for Pin 8 From: SC2 To: SD2 in the <i>Pin Functions</i> table.....	3
• Added the <i>Typical Characteristics</i> section.....	10
Changes from Revision D (June 2014) to Revision E (February 2015)	Page
• 更改了首页图.....	1
• Added <i>Thermal Information</i> .	5
• Changed Note <sup>(2)</sup> in the <i>Electrical Characteristics</i>	6
• Added <i>Layout Example</i> .....	27
Changes from Revision C (June 2007) to Revision D (June 2014)	Page
• Added RESET Errata section.....	15
• Updated Typical Application schematic.	20

## 5 Pin Configuration and Functions

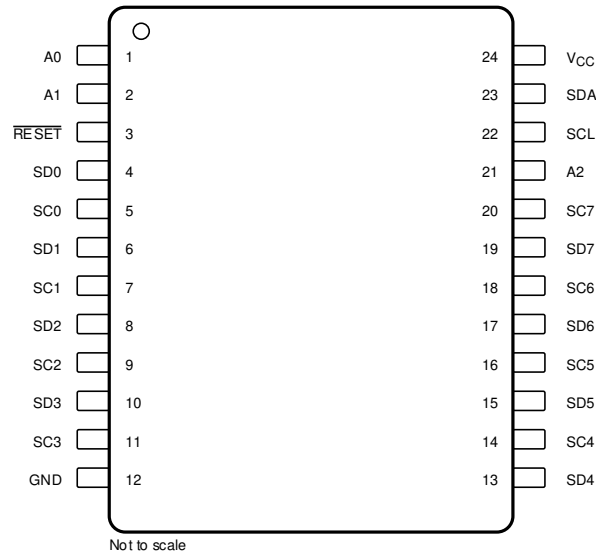


图 5-1. DB, DGV, DW or PW Package, 24-Pin SSOP, TVSOP, SOIC or TSSOP , Top View

表 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	NO.	DB, DW, DGV, PW		
A0	1		I	Address input 0. Connect directly to $V_{CC}$ or ground
A1	2		I	Address input 1. Connect directly to $V_{CC}$ or ground
RESET	3		I	Active-low reset input. Connect to $V_{CC}$ through a pull-up resistor, if not used
SD0	4		I/O	Serial data 0. Connect to $V_{CC}$ through a pull-up resistor
SC0	5		I/O	Serial clock 0. Connect to $V_{CC}$ through a pull-up resistor
SD1	6		I/O	Serial data 1. Connect to $V_{CC}$ through a pull-up resistor
SC1	7		I/O	Serial clock 1. Connect to $V_{CC}$ through a pull-up resistor
SD2	8		I/O	Serial data 2. Connect to $V_{CC}$ through a pull-up resistor
SC2	9		I/O	Serial clock 2. Connect to $V_{CC}$ through a pull-up resistor
SD3	10		I/O	Serial data 3. Connect to $V_{CC}$ through a pull-up resistor
SC3	11		I/O	Serial clock 3. Connect to $V_{CC}$ through a pull-up resistor
GND	12		—	Ground
SD4	13		I/O	Serial data 4. Connect to $V_{CC}$ through a pull-up resistor
SC4	14		I/O	Serial clock 4. Connect to $V_{CC}$ through a pull-up resistor
SD5	15		I/O	Serial data 5. Connect to $V_{CC}$ through a pull-up resistor
SC5	16		I/O	Serial clock 5. Connect to $V_{CC}$ through a pull-up resistor
SD6	17		I/O	Serial data 6. Connect to $V_{CC}$ through a pull-up resistor
SC6	18		I/O	Serial clock 6. Connect to $V_{CC}$ through a pull-up resistor
SD7	19		I/O	Serial data 7. Connect to $V_{CC}$ through a pull-up resistor
SC7	20		I/O	Serial clock 7. Connect to $V_{CC}$ through a pull-up resistor
A2	21		I	Address input 2. Connect directly to $V_{CC}$ or ground
SCL	22		I/O	Serial clock bus. Connect to $V_{CC}$ through a pull-up resistor
SDA	23		I/O	Serial data bus. Connect to $V_{CC}$ through a pull-up resistor
$V_{CC}$	24		—	Supply voltage

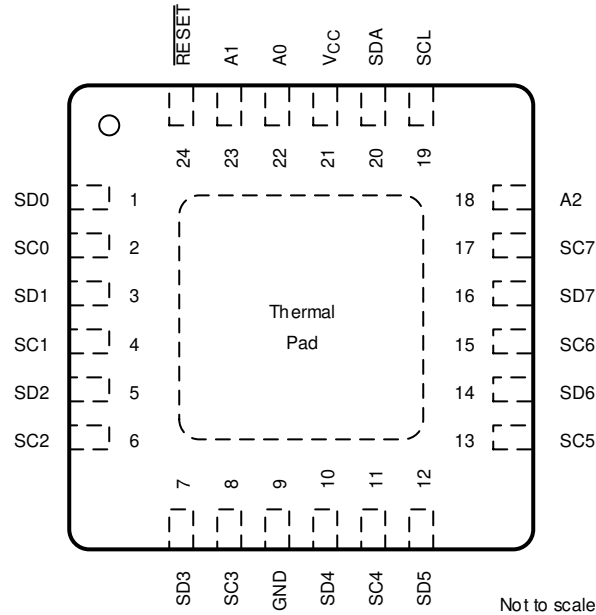


图 5-2. RGE Package, 24-Pin VQFN , Top View

表 5-2. Pin Functions, RGE

PIN		I/O	DESCRIPTION
NAME	NO.		
SD0	1	I/O	Serial data 0. Connect to $V_{CC}$ through a pull-up resistor
SC0	2	I/O	Serial clock 0. Connect to $V_{CC}$ through a pull-up resistor
SD1	3	I/O	Serial data 1. Connect to $V_{CC}$ through a pull-up resistor
SC1	4	I/O	Serial clock 1. Connect to $V_{CC}$ through a pull-up resistor
SD2	5	I/O	Serial data 2. Connect to $V_{CC}$ through a pull-up resistor
SC2	6	I/O	Serial clock 2. Connect to $V_{CC}$ through a pull-up resistor
SD3	7	I/O	Serial data 3. Connect to $V_{CC}$ through a pull-up resistor
SC3	8	I/O	Serial clock 3. Connect to $V_{CC}$ through a pull-up resistor
GND	9	—	Ground
SD4	10	I/O	Serial data 4. Connect to $V_{CC}$ through a pull-up resistor
SC4	11	I/O	Serial clock 4. Connect to $V_{CC}$ through a pull-up resistor
SD5	12	I/O	Serial data 5. Connect to $V_{CC}$ through a pull-up resistor
SC5	13	I/O	Serial clock 5. Connect to $V_{CC}$ through a pull-up resistor
SD6	14	I/O	Serial data 6. Connect to $V_{CC}$ through a pull-up resistor
SC6	15	I/O	Serial clock 6. Connect to $V_{CC}$ through a pull-up resistor
SD7	16	I/O	Serial data 7. Connect to $V_{CC}$ through a pull-up resistor
SC7	17	I/O	Serial clock 7. Connect to $V_{CC}$ through a pull-up resistor
A2	18	I	Address input 2. Connect directly to $V_{CC}$ or ground
SCL	19	I/O	Serial clock bus. Connect to $V_{CC}$ through a pull-up resistor
SDA	20	I/O	Serial data bus. Connect to $V_{CC}$ through a pull-up resistor
$V_{CC}$	21	—	Supply voltage
A0	22	I	Address input 0. Connect directly to $V_{CC}$ or ground
A1	23	I	Address input 1. Connect directly to $V_{CC}$ or ground
RESET	24	I	Active-low reset input. Connect to $V_{CC}$ through a pull-up resistor, if not used

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	- 0.5	7	V
I <sub>I</sub>	Input current	- 20	20	mA
I <sub>O</sub>	Output current	- 25	25	mA
I <sub>CC</sub>	Supply current	- 100	100	mA
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5.5	V
V <sub>IH</sub>	High-level input voltage	SCL, SDA	0.7 × V <sub>CC</sub>	6
		A2 - A0, RESET	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.5
V <sub>IL</sub>	Low-level input voltage	SCL, SDA	- 0.5	0.3 × V <sub>CC</sub>
		A2 - A0, RESET	- 0.5	0.3 × V <sub>CC</sub>
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the [Implications of Slow or Floating CMOS Inputs](#) application report.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	PCA9548A					UNIT	
	DB (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	RGE (VQFN)		
	24 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	89.1	99.6	73.2	108.8	57.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	51.1	31.1	41.3	54.1	62.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	46.6	53.1	42.9	62.7	34.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.5	0.9	15.3	10.9	3.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.3	52.6	42.6	62.3	34.4	°C/W

## 6.4 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>	PCA9548A					UNIT
	DB (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	RGE (VQFN)	
	24 PINS					
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

$V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$ , over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{PORR}$	Power-on reset voltage, $V_{CC}$ rising	No load, $V_I = V_{CC}$ or GND			1.2	1.5	V	
$V_{PORF}$	Power-on reset voltage, $V_{CC}$ falling <sup>(2)</sup>	No load, $V_I = V_{CC}$ or GND		0.8	1		V	
$V_{O(sw)}$	Switch output voltage	$V_{i(sw)} = V_{CC}$ , $I_{SWout} = -100 \mu\text{A}$	5 V		3.6		V	
			4.5 V to 5.5 V	2.6		4.5		
			3.3 V		1.9			
			3 V to 3.6 V	1.6		2.8		
			2.5 V		1.5			
			2.3 V to 2.7 V	1.1		2		
$I_{OL}$	SDA	$V_{OL} = 0.4 \text{ V}$	2.3 V to 5.5 V	3		6	mA	
		$V_{OL} = 0.6 \text{ V}$		6		9		
$I_I$	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V	-1		1	$\mu\text{A}$	
	SC7 - SC0, SD7 - SD0			-1		1		
	A2 - A0			-1		1		
	RESET			-1		1		
$I_{CC}$	Operating mode	$f_{SCL} = 400 \text{ kHz}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		50	80	$\mu\text{A}$
				3.6 V		20	35	
				2.7 V		11	20	
		5.5 V			9	30		
		3.6 V			6	15		
		2.7 V			4	8		
	Standby mode	Low inputs	$V_I = \text{GND}$ , $I_O = 0$	5.5 V		0.2	2	
				3.6 V		0.1	2	
		2.7 V			0.1	1		
		High inputs		$V_I = V_{CC}$ , $I_O = 0$	5.5 V		0.2	
3.6 V			0.1		2			
		2.7 V		0.1	1			
$\Delta I_{CC}$	Supply-current change	SCL, SDA	2.3 V to 5.5 V	SCL or SDA input at 0.6 V, Other inputs at $V_{CC}$ or GND		3	20	$\mu\text{A}$
				SCL or SDA input at $V_{CC} - 0.6 \text{ V}$ , Other inputs at $V_{CC}$ or GND		3	20	
$C_i$	A2 - A0	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			4	5	pF
	RESET					4	5	
	SCL			$V_I = V_{CC}$ or GND, Switch OFF		20	28	
$C_{io(off)}$ <sup>(3)</sup>	SDA	$V_I = V_{CC}$ or GND, Switch OFF	2.3 V to 5.5 V			20	28	pF
	SC7 - SC0, SD7 - SD0					5.5	7.5	

## 6.5 Electrical Characteristics (continued)

$V_{CC} = 2.3\text{ V to }3.6\text{ V}$ , over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$V_{CC}$	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$R_{ON}$	Switch-on resistance	$V_O = 0.4\text{ V}$ , $I_O = 15\text{ mA}$	4.5 V to 5.5 V	4	10	20	$\Omega$
			3 V to 3.6 V	5	12	30	
		$V_O = 0.4\text{ V}$ , $I_O = 10\text{ mA}$	2.3 V to 2.7 V	7	15	45	

- (1) All typical values are at nominal supply voltage (2.5-, 3.3-, or 5-V  $V_{CC}$ ),  $T_A = 25^\circ\text{C}$ .
- (2) The power-on reset circuit resets the I<sup>2</sup>C bus logic with  $V_{CC} < V_{PORF}$ .
- (3)  $C_{iO(ON)}$  depends on internal capacitance and external capacitance added to the SCn lines when channel(s) are ON.

## 6.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 图 7-1)

		MIN	MAX	UNIT
<b>STANDARD MODE</b>				
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	100	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	4		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	4.7		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	250		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		μs
t <sub>icr</sub>	I <sup>2</sup> C input rise time		1000	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time		300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output (SDn) fall time (10-pF to 400-pF bus)		300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	4.7		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	4.7		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	4		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	4		μs
t <sub>vdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid		1 μs
t <sub>vdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid		0.6 μs
t <sub>vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1 μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF
<b>FAST MODE</b>				
f <sub>scl</sub>	I <sup>2</sup> C clock frequency	0	400	kHz
t <sub>sch</sub>	I <sup>2</sup> C clock high time	0.6		μs
t <sub>scl</sub>	I <sup>2</sup> C clock low time	1.3		μs
t <sub>sp</sub>	I <sup>2</sup> C spike time		50	ns
t <sub>sds</sub>	I <sup>2</sup> C serial-data setup time	100		ns
t <sub>sdh</sub>	I <sup>2</sup> C serial-data hold time	0 <sup>(1)</sup>		μs
t <sub>icr</sub>	I <sup>2</sup> C input rise time	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>icf</sub>	I <sup>2</sup> C input fall time	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>ocf</sub>	I <sup>2</sup> C output (SDn) fall time (10-pF to 400-pF bus)	20 + 0.1C <sub>b</sub> <sup>(2)</sup>	300	ns
t <sub>buf</sub>	I <sup>2</sup> C bus free time between stop and start	1.3		μs
t <sub>sts</sub>	I <sup>2</sup> C start or repeated start condition setup	0.6		μs
t <sub>sth</sub>	I <sup>2</sup> C start or repeated start condition hold	0.6		μs
t <sub>sps</sub>	I <sup>2</sup> C stop condition setup	0.6		μs
t <sub>vdL(Data)</sub>	Valid-data time (high to low) <sup>(3)</sup>	SCL low to SDA output low valid		1 μs
t <sub>vdH(Data)</sub>	Valid-data time (low to high) <sup>(3)</sup>	SCL low to SDA output high valid		0.6 μs
t <sub>vd(ack)</sub>	Valid-data time of ACK condition	ACK signal from SCL low to SDA output low		1 μs
C <sub>b</sub>	I <sup>2</sup> C bus capacitive load		400	pF

(1) A device internally must provide a hold time of at least 300 ns for the SDA signal (referred to the V<sub>IH</sub> min of the SCL signal), to bridge the undefined region of the falling edge of SCL.

(2) C<sub>b</sub> = total bus capacitance of one bus line in pF.

(3) Data taken using a 1-kΩ pull-up resistor and 50-pF load (see 图 7-2).

## 6.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$t_{W(L)}$	Pulse duration, RESET low	6		ns
$t_{REC(STA)}$	Recovery time from RESET to start	0		ns

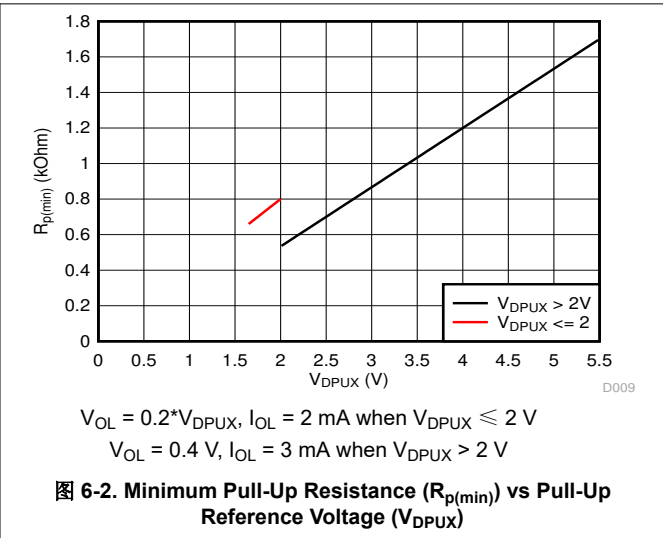
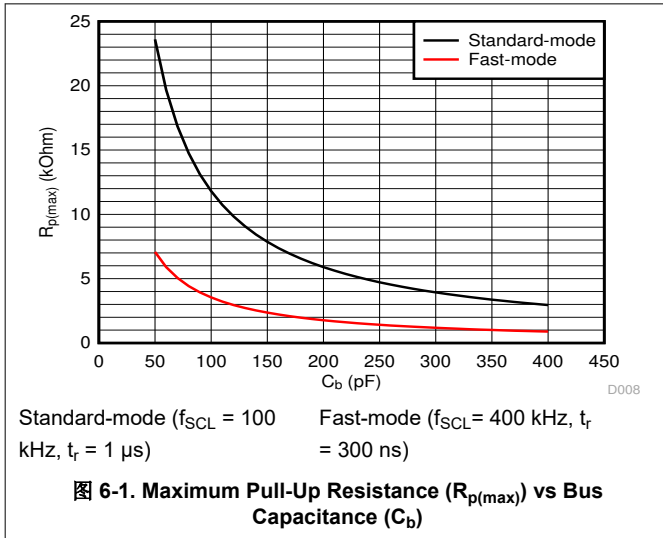
## 6.8 Switching Characteristics

over recommended operating free-air temperature range,  $C_L \leq 100$  pF (unless otherwise noted) (see [图 7-1](#))

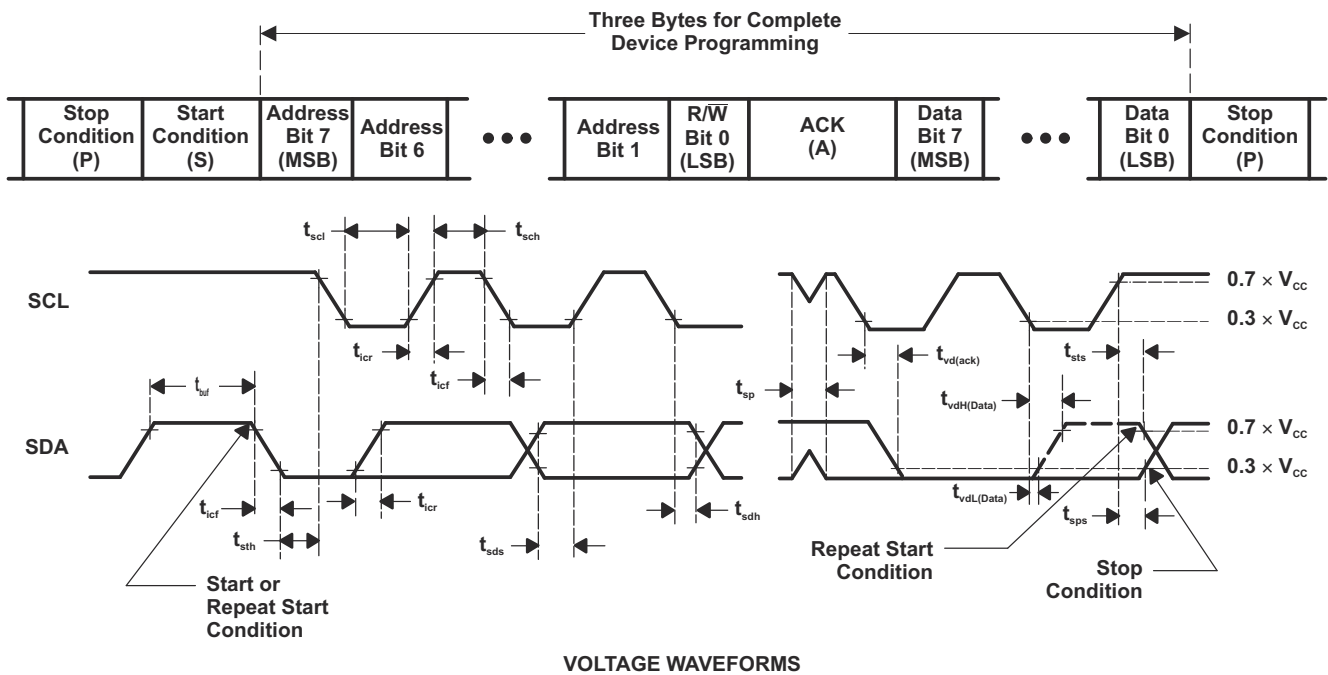
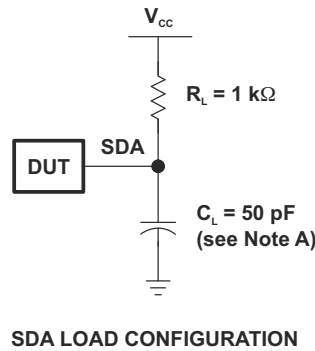
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
$t_{pd}$ (1)	Propagation delay time	$R_{ON} = 20 \Omega$ , $C_L = 15$ pF	SDA or SCL	SDn or SCn	0.3	ns
		$R_{ON} = 20 \Omega$ , $C_L = 50$ pF	SDA or SCL	SDn or SCn	1	
$t_{rst}$ (2)	RESET time (SDA clear)	RESET	SDA	500		ns

- (1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- (2)  $t_{rst}$  is the propagation delay measured from the time the RESET pin is first asserted low to the time the SDA pin is asserted high, signaling a stop condition. It must be a minimum of  $t_{WL}$ .

### 6.9 Typical Characteristics



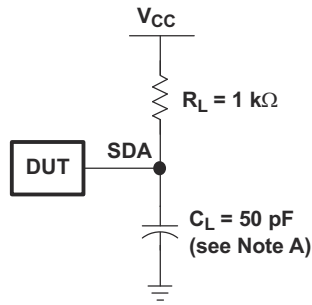
## 7 Parameter Measurement Information



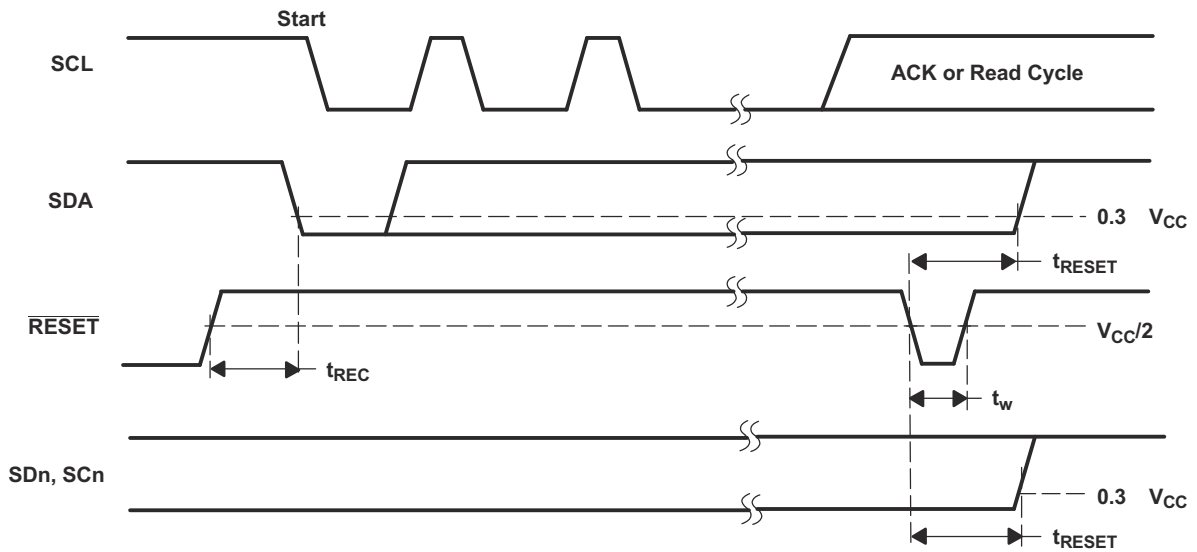
BYTE	DESCRIPTION
1	I <sup>2</sup> C address
2, 3	P-port data

- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30$  ns.
- C. Not all parameters and waveforms are applicable to all devices.

**图 7-1. I<sup>2</sup>C Load Circuit and Voltage Waveforms**



SDA LOAD CONFIGURATION



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.
- C. I/Os are configured as inputs.
- D. Not all parameters and waveforms are applicable to all devices.

图 7-2. Reset Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

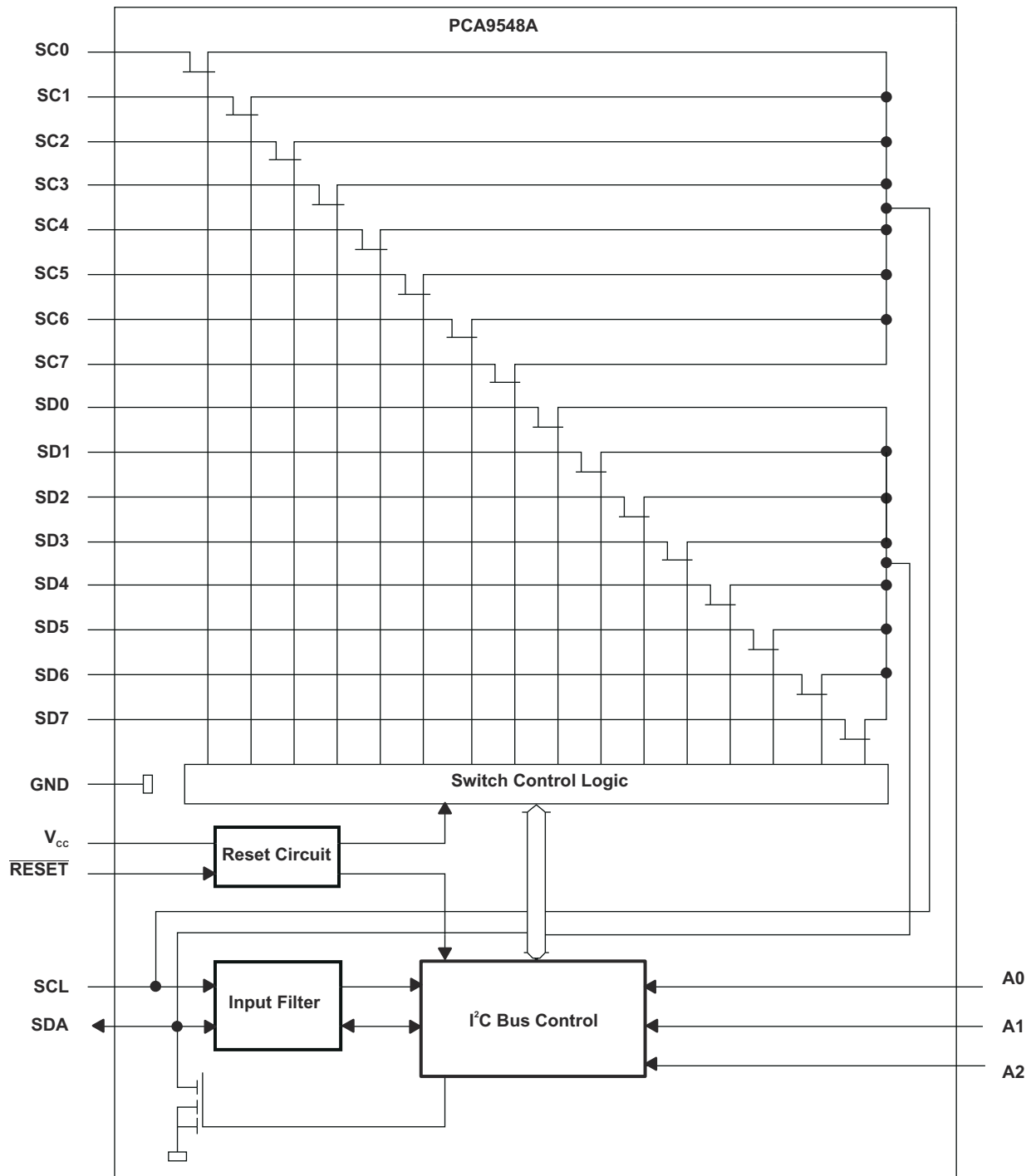
The PCA9548A is a 8-channel, bidirectional translating I<sup>2</sup>C switch. The master SCL/SDA signal pair is directed to eight channels of slave devices, SC0/SD0-SC3/SD3. Any individual downstream channel can be selected as well as any combination of the eight channels.

The device offers an active-low  $\overline{\text{RESET}}$  input which resets the state machine and allows the PCA9548A to recover if one of the downstream I<sup>2</sup>C buses get stuck in a low state. The state machine of the device can also be reset by cycling the power supply, V<sub>CC</sub>, also known as a power-on reset (POR). Both the  $\overline{\text{RESET}}$  function and a POR cause all channels to be deselected.

The connections of the I<sup>2</sup>C data path are controlled by the same I<sup>2</sup>C master device that is switched to communicate with multiple I<sup>2</sup>C slaves. After the successful acknowledgment of the slave address (hardware selectable by A0 and A1 pins), a single 8-bit control register is written to or read from to determine the selected channels.

The PCA9548A may also be used for voltage translation, allowing the use of different bus voltages on each SC<sub>n</sub>/SD<sub>n</sub> pair such that 1.8-V, 2.5-V, or 3.3-V parts can communicate with 5-V parts. This is achieved by using external pull-up resistors to pull the bus up to the desired voltage for the master and each slave channel.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

The PCA9548A is an 8-channel, bidirectional translating switch for I<sup>2</sup>C buses that supports Standard-Mode (100 kHz) and Fast-Mode (400 kHz) operation. The PCA9548A features I<sup>2</sup>C control using a single 8-bit control register in which each bit controls the enabling and disabling for one of the 8 switch channels of I<sup>2</sup>C data flow. Depending on the application, voltage translation of the I<sup>2</sup>C bus can also be achieved using the PCA9548A to allow 1.8-V, 2.5-V, or 3.3-V parts to communicate with 5-V parts. Additionally, in the event that communication on the I<sup>2</sup>C bus enters a fault state, the PCA9548A can be reset to resume normal operation using the RESET pin feature or by a power-on reset which results from cycling power to the device.

## 8.4 Device Functional Modes

### 8.4.1 RESET Input

The  $\overline{\text{RESET}}$  input is an active-low signal that may be used to recover from a bus-fault condition. When this signal is asserted low for a minimum of  $t_{WL}$ , the PCA9548A resets its registers and I<sup>2</sup>C state machine and deselects all channels. The  $\overline{\text{RESET}}$  input must be connected to  $V_{CC}$  through a pull-up resistor.

#### 8.4.1.1 $\overline{\text{RESET}}$ Errata

If RESET voltage set higher than VCC, current flows from RESET pin to VCC pin.

##### 8.4.1.1.1 System Impact

VCC is pulled above its regular voltage level.

##### 8.4.1.1.2 System Workaround

Design such that  $\overline{\text{RESET}}$  voltage is same or lower than VCC.

### 8.4.2 Power-On Reset

When power (from 0 V) is applied to  $V_{CC}$ , an internal power-on reset holds the PCA9548A in a reset condition until  $V_{CC}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9548A registers and I<sup>2</sup>C state machine initialize to their default states. After that,  $V_{CC}$  must be lowered to below  $V_{POR}$  and then back up to the operating voltage for a power-reset cycle.

## 8.5 Programming

### 8.5.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 8-1](#)). After the start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$ ).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 - A2) of the slave device must not be changed between the start and the stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see [Figure 8-2](#)).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see [Figure 8-1](#)).

Any number of data bytes can be transferred from the transmitter to receiver between the start and the stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 8-3](#)). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

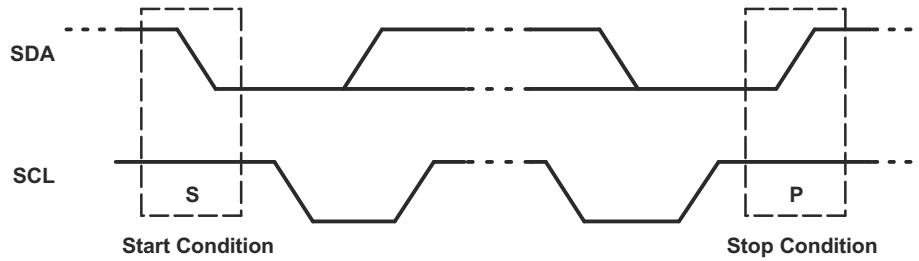


图 8-1. Definition of Start and Stop Conditions

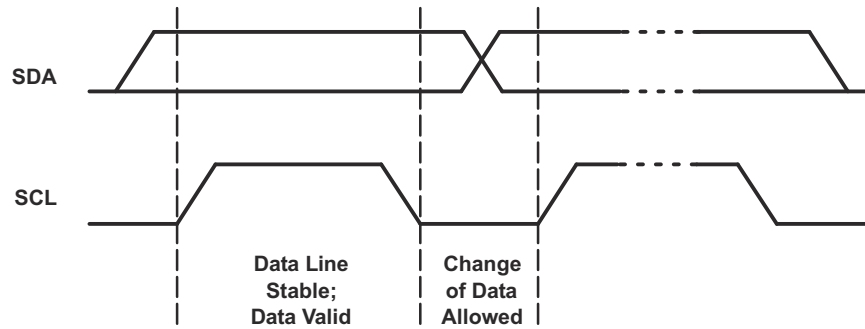


图 8-2. Bit Transfer

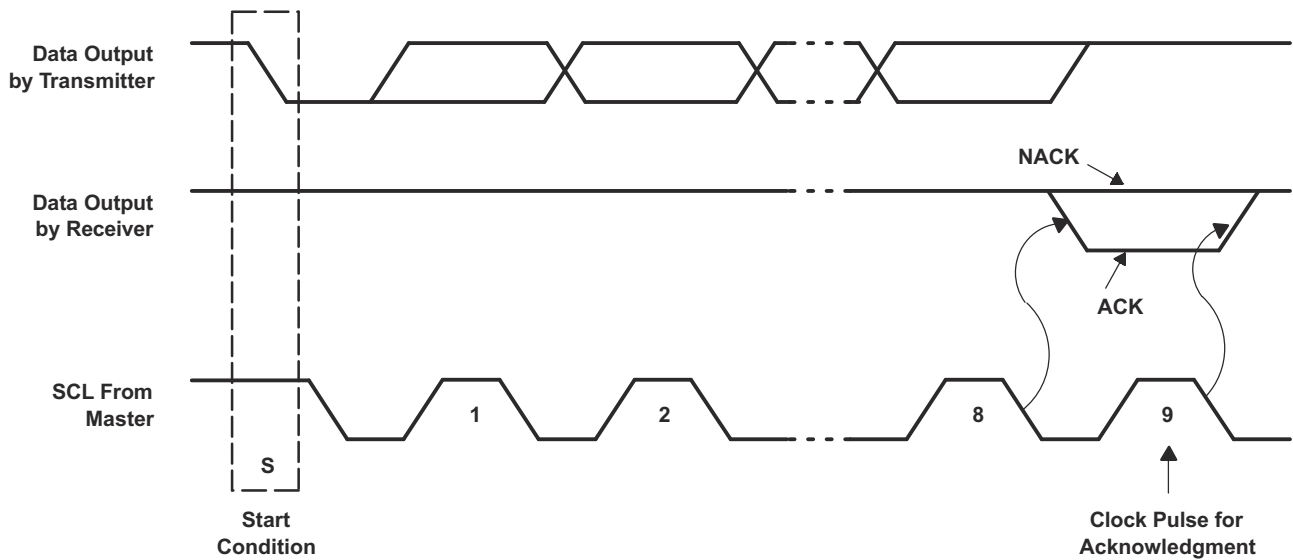


图 8-3. Acknowledgment on I<sup>2</sup>C Bus

## 8.6 Register Maps

### 8.6.1 Device Address

图 8-4 shows the address byte of the PCA9548A.

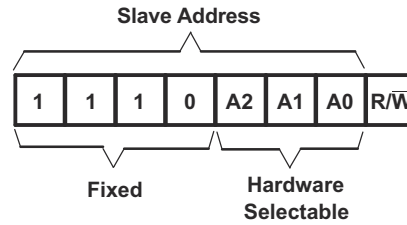


图 8-4. PCA9548A Address

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

表 8-1 shows the PCA9548A address reference.

表 8-1. Address Reference

INPUTS			I <sup>2</sup> C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	112 (decimal), 70 (hexadecimal)
L	L	H	113 (decimal), 71 (hexadecimal)
L	H	L	114 (decimal), 72 (hexadecimal)
L	H	H	115 (decimal), 73 (hexadecimal)
H	L	L	116 (decimal), 74 (hexadecimal)
H	L	H	117 (decimal), 75 (hexadecimal)
H	H	L	118 (decimal), 76 (hexadecimal)
H	H	H	119 (decimal), 77 (hexadecimal)

### 8.6.2 Control Register

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9548A (see 图 8-5). This register can be written and read via the I<sup>2</sup>C bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high (or 1) selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I<sup>2</sup>C bus. This ensures that all SCn/SDn lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle. If multiple bytes are received by the PCA9548A, it saves the last byte received.

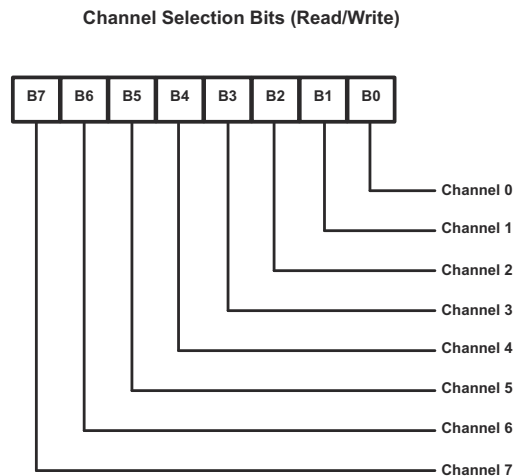


图 8-5. Control Register

表 8-2 shows the PCA9548A Command byte definition.

表 8-2. Command Byte Definition

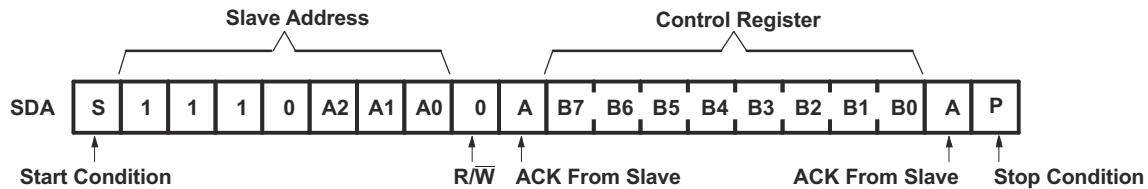
CONTROL REGISTER BITS								COMMAND
B7	B6	B5	B4	B3	B2	B1	B0	
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	X	0	Channel 1 disabled
							1	Channel 1 enabled
X	X	X	X	X	X	X	0	Channel 2 disabled
							1	Channel 2 enabled
X	X	X	X	X	X	X	0	Channel 3 disabled
							1	Channel 3 enabled
X	X	X	X	X	X	X	0	Channel 4 disabled
							1	Channel 4 enabled
X	X	X	X	X	X	X	0	Channel 5 disabled
							1	Channel 5 enabled
X	X	X	X	X	X	X	0	Channel 6 disabled
							1	Channel 6 enabled
0	X	X	X	X	X	X	0	Channel 7 disabled
							1	Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

### 8.6.3 Bus Transactions

Data is exchanged between the master and PCA9548A through write and read commands.

#### 8.6.3.1 Writes

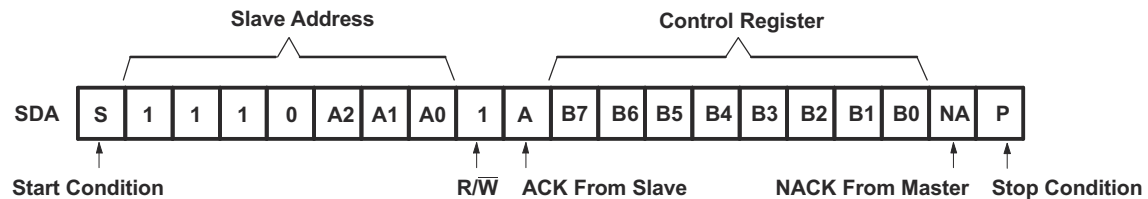
Data is transmitted to the PCA9548A by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see [图 8-4](#) for device address). The command byte is sent after the address and determines which SCn/SDn channel receives the data that follows the command byte (see [图 8-6](#)). There is no limitation on the number of data bytes sent in one write transmission.



**图 8-6. Write to Control Register**

#### 8.6.3.2 Reads

The bus master first must send the PCA9548A address with the LSB set to a logic 1 (see [图 8-4](#) for device address). The command byte is sent after the address and determines which SCn/SDn channel is accessed. After a restart, the device address is sent again, but this time, the LSB is set to a logic 1. Data from the SCn/SDn channel defined by the command byte then is sent by the PCA9548A (see [图 8-7](#)). After a restart, the value of the SCn/SDn channel defined by the command byte matches the SCn/SDn channel being accessed when the restart occurred. Data is clocked into the SCn/SDn channel on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.



**图 8-7. Read From Control Register**

## 9 Application Information Disclaimer

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

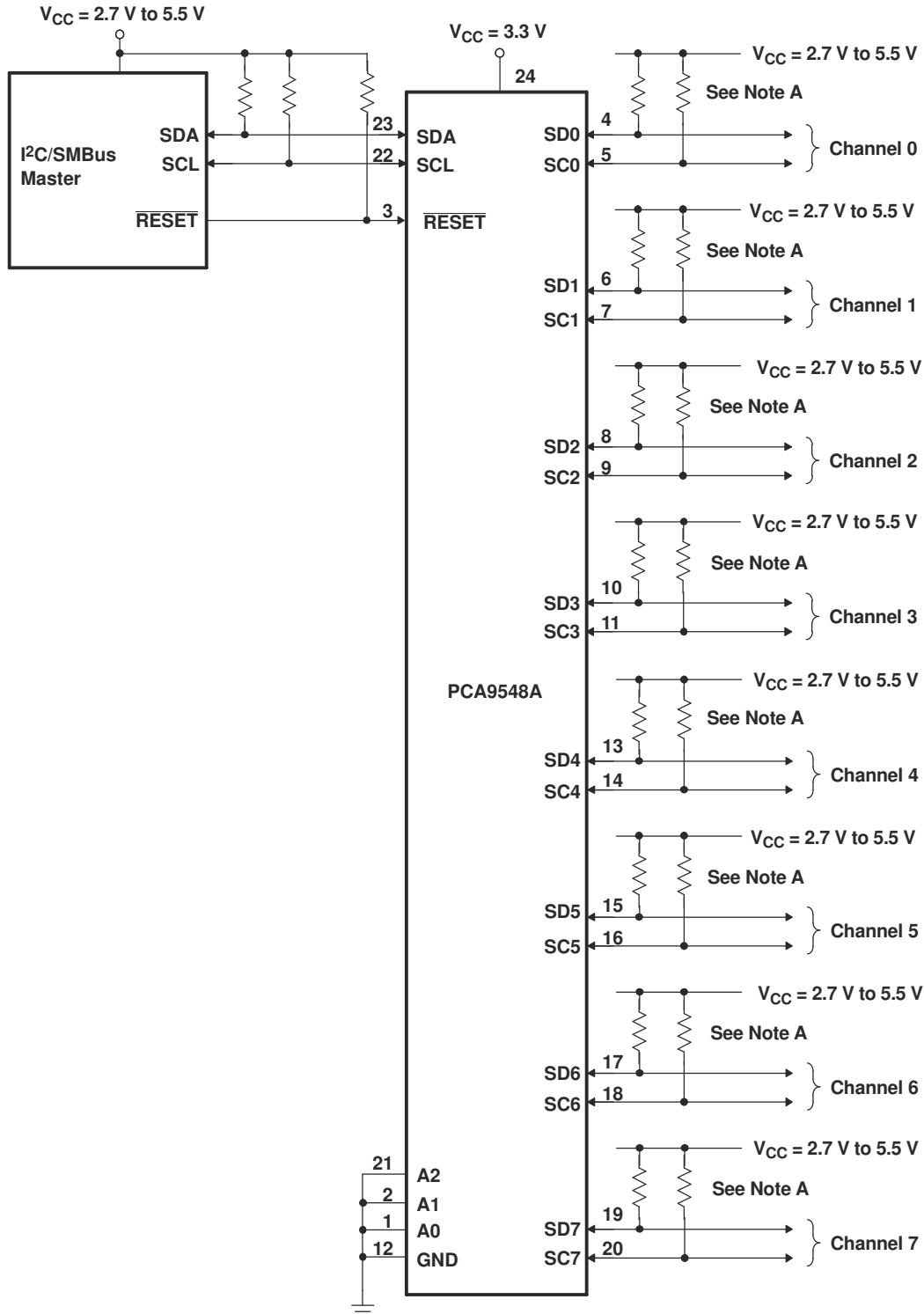
Applications of the PCA9548A contain an I<sup>2</sup>C (or SMBus) master device and up to eight I<sup>2</sup>C slave devices. The downstream channels are ideally used to resolve I<sup>2</sup>C slave address conflicts. For example, if eight identical digital temperature sensors are needed in the application, one sensor can be connected at each channel: 0, 1, 2, and 3. When the temperature at a specific location needs to be read, the appropriate channel can be enabled and all other channels switched off, the data can be retrieved, and the I<sup>2</sup>C master can move on and read the next channel.

In an application where the I<sup>2</sup>C bus contains many additional slave devices that do not result in I<sup>2</sup>C slave address conflicts, these slave devices can be connected to any desired channel to distribute the total bus capacitance across multiple channels. If multiple switches are enabled simultaneously, additional design requirements must be considered (See the [Design Requirements](#) and [Detailed Design Procedure](#) sections).

### 9.2 Typical Application

A typical application of the PCA9548A contains 1 or many separate data pull-up voltages,  $V_{CC}$ , one for the master device and one for each of the selectable slave channels, 0 through 7. In the event where the master device and all slave devices operate at the same voltage, then the VCC pin can be connected to this supply voltage. In an application where voltage translation is necessary, additional design requirements must be considered (See the [Design Requirements](#) section).

 [9-1](#) shows an application in which the PCA9548A can be used.



A. Pin numbers shown are for the PW and RTW packages.

图 9-1. PCA9548A Typical Application Schematic

### 9.2.1 Design Requirements

The A0, A1, and A2 pins are hardware selectable to control the slave address of the PCA9548A. These pins may be tied directly to GND or  $V_{CC}$  in the application.

If multiple slave channels are activated simultaneously in the application, then the total  $I_{OL}$  from SCL/SDA to GND on the master side is the sum of the currents through all pull-up resistors,  $R_p$ .

The pass-gate transistors of the PCA9548A are constructed such that the  $V_{CC}$  voltage can be used to limit the maximum voltage that is passed from one I<sup>2</sup>C bus to another.

[Pass-Gate Voltage \( \$V\_{pass}\$ \) vs Supply Voltage \( \$V\_{CC}\$ \) at Three Temperature Points](#) shows the voltage characteristics of the pass-gate transistors (note that the graph was generated using data specified in the [Electrical Characteristics](#) section of this data sheet). In order for the PCA9548A to act as a voltage translator, the  $V_{pass}$  voltage must be equal to or lower than the lowest bus voltage. For example, if the main bus is running at 5 V and the downstream buses are 3.3 V and 2.7 V,  $V_{pass}$  must be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in [Pass-Gate Voltage \( \$V\_{pass}\$ \) vs Supply Voltage \( \$V\_{CC}\$ \) at Three Temperature Points](#),  $V_{pass(max)}$  is 2.7 V when the PCA9548A supply voltage is 4 V or lower, so the PCA9548A supply voltage could be set to 3.3 V. Pull-up resistors then can be used to bring the bus voltages to their appropriate levels (see [图 9-1](#)).

### 9.2.2 Detailed Design Procedure

Once all the slaves are assigned to the appropriate slave channels and bus voltages are identified, the pull-up resistors,  $R_p$ , for each of the buses need to be selected appropriately. The minimum pull-up resistance is a function of the reference voltage of the specific I<sup>2</sup>C channel ( $V_{DPUX}$ ),  $V_{OL(max)}$ , and  $I_{OL}$  as shown in [方程式 1](#).

$$R_{p(min)} = \frac{V_{DPUX} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time,  $t_r$  (300 ns for fast-mode operation,  $f_{SCL} = 400$  kHz) and bus capacitance,  $C_b$  is given by [方程式 2](#).

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I<sup>2</sup>C bus must not exceed 400 pF for fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCA9548A,  $C_{io(OFF)}$ , the capacitance of wires, connections, traces, and the capacitance of each individual slave on a given channel. If multiple channels are activated simultaneously, each of the slaves on all channels contribute to total bus capacitance.

### 9.2.3 Application Curves

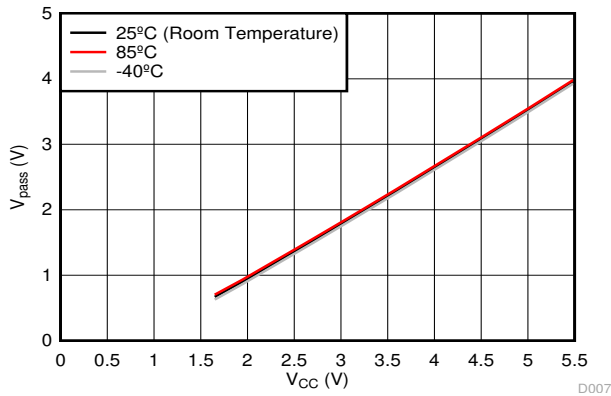
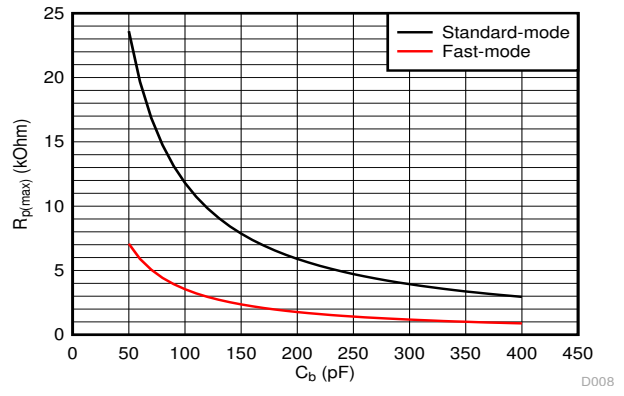
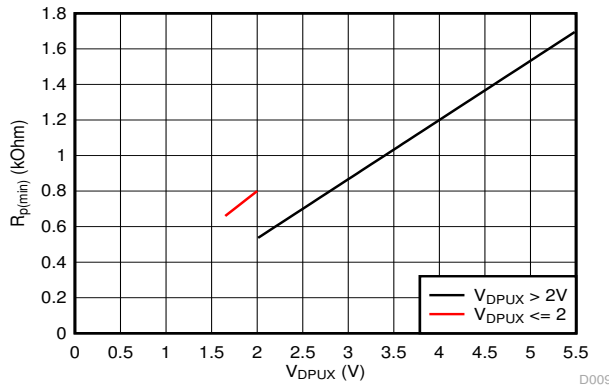


图 9-2. Pass-Gate Voltage ( $V_{pass}$ ) vs Supply Voltage ( $V_{CC}$ ) at Three Temperature Points



Standard-mode ( $f_{SCL} = 100$  kHz,  $t_r = 1 \mu s$ )      Fast-mode ( $f_{SCL} = 400$  kHz,  $t_r = 300$  ns)

图 9-3. Maximum Pull-Up Resistance ( $R_{p(max)}$ ) vs Bus Capacitance ( $C_b$ )



$$V_{OL} = 0.2 \cdot V_{DPUX}, I_{OL} = 2 \text{ mA when } V_{DPUX} \leq 2 \text{ V}$$

$$V_{OL} = 0.4 \text{ V}, I_{OL} = 3 \text{ mA when } V_{DPUX} > 2 \text{ V}$$

图 9-4. Minimum Pullup Resistance ( $R_{p(min)}$ ) vs Pullup Reference Voltage ( $V_{DPUX}$ )

## 10 Power Supply Recommendations

### 10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9548A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 10-1 and 图 10-2.

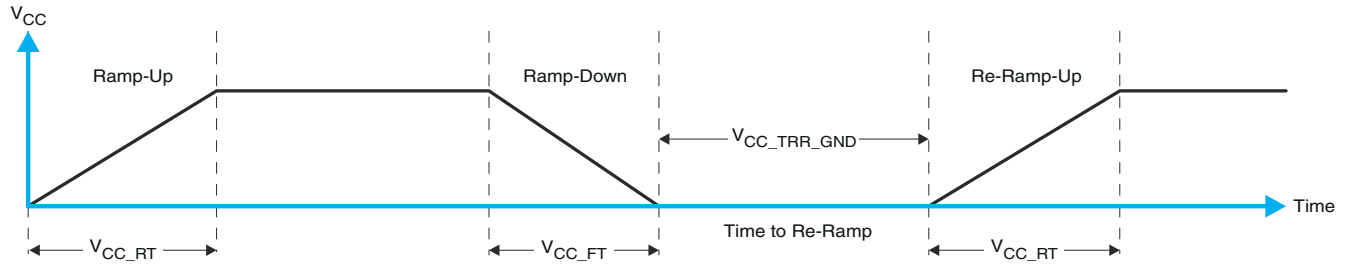


图 10-1.  $V_{CC}$  Is Lowered Below 0.2 V or 0 V and Then Ramped Up To  $V_{CC}$

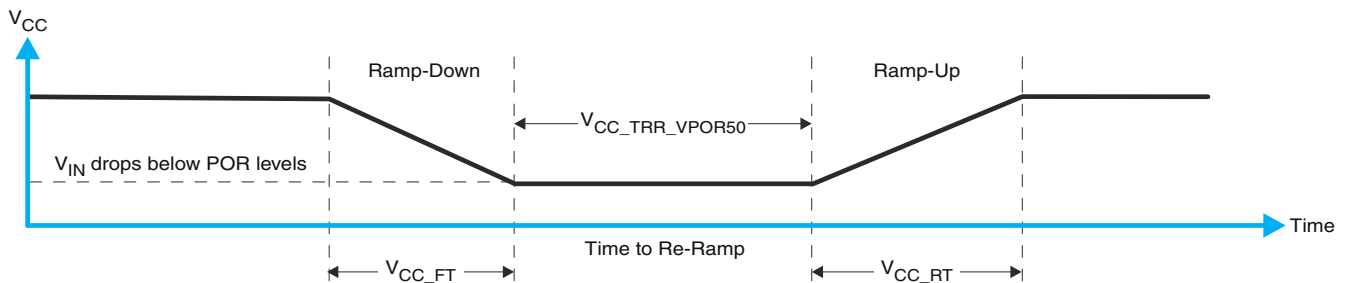


图 10-2.  $V_{CC}$  Is Lowered Below The Por Threshold, Then Ramped Back Up To  $V_{CC}$

表 10-1 specifies the performance of the power-on reset feature for PCA9548A for both types of power-on reset.

表 10-1. Recommended Supply Sequencing And Ramp Rates<sup>(1)</sup>

PARAMETER			MIN	TYP	MAX	UNIT
$V_{CC\_FT}$	Fall rate	See 图 10-1	1		100	ms
$V_{CC\_RT}$	Rise rate	See 图 10-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when $V_{CC}$ drops to GND)	See 图 10-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when $V_{CC}$ drops to $V_{POR\_MIN} - 50$ mV)	See 图 10-2	0.001			ms
$V_{CC\_GH}$	Level that $V_{CCP}$ can glitch down to, but not cause a functional disruption when $V_{CCX\_GW} = 1$ $\mu$ s	See 图 10-3			1.2	V
$V_{CC\_GW}$	Glitch width that will not cause a functional disruption when $V_{CCX\_GH} = 0.5 \times V_{CCX}$	See 图 10-3				$\mu$ s
$V_{PORF}$	Voltage trip point of POR on falling $V_{CC}$		0.767		1.144	V
$V_{PORR}$	Voltage trip point of POR on rising $V_{CC}$		1.033		1.428	V

(1)  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$  (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $V_{CC\_GW}$ ) and height ( $V_{CC\_GH}$ ) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 图 10-3 and 表 10-1 provide more information on how to measure these specifications.

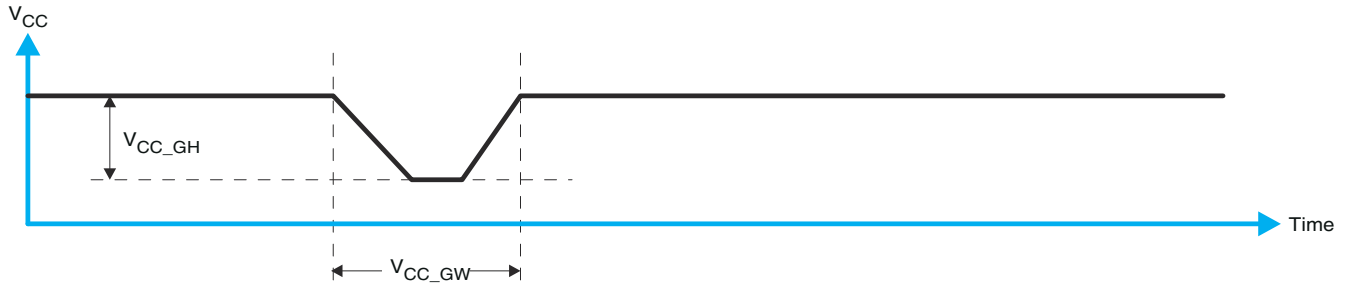


图 10-3. Glitch Width And Glitch Height

$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{CC}$  being lowered to or from 0. 图 10-4 和 表 10-1 提供更多信息。

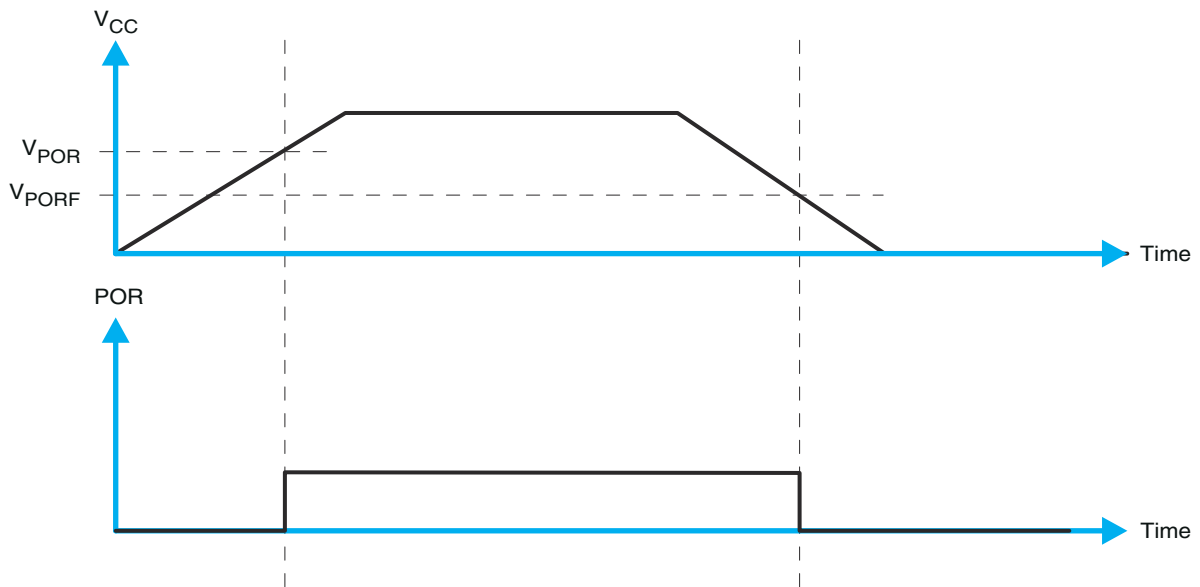


图 10-4.  $V_{POR}$

## 11 Layout

### 11.1 Layout Guidelines

For PCB layout of the PCA9548A, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I<sup>2</sup>C signal speeds. It is common to have a dedicated ground plane on an inner layer of the board and pins that are connected to ground must have a low-impedance path to the ground plane in the form of wide polygon pours and multiple vias. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple.

In an application where voltage translation is not required, all V<sub>DPUX</sub> voltages and V<sub>CC</sub> could be at the same potential and a single copper plane could connect all of pull-up resistors to the appropriate reference voltage. In an application where voltage translation is required, V<sub>DPU0</sub> and V<sub>DPU0</sub> - V<sub>DPU7</sub> may all be on the same layer of the board with split planes to isolate different voltage potentials.

To reduce the total I<sup>2</sup>C bus capacitance added by PCB parasitics, data lines (SC<sub>n</sub> and SD<sub>n</sub>) must be as short as possible and the widths of the traces must also be minimized (For example, 5-10 mils depending on copper weight).

## 11.2 Layout Example

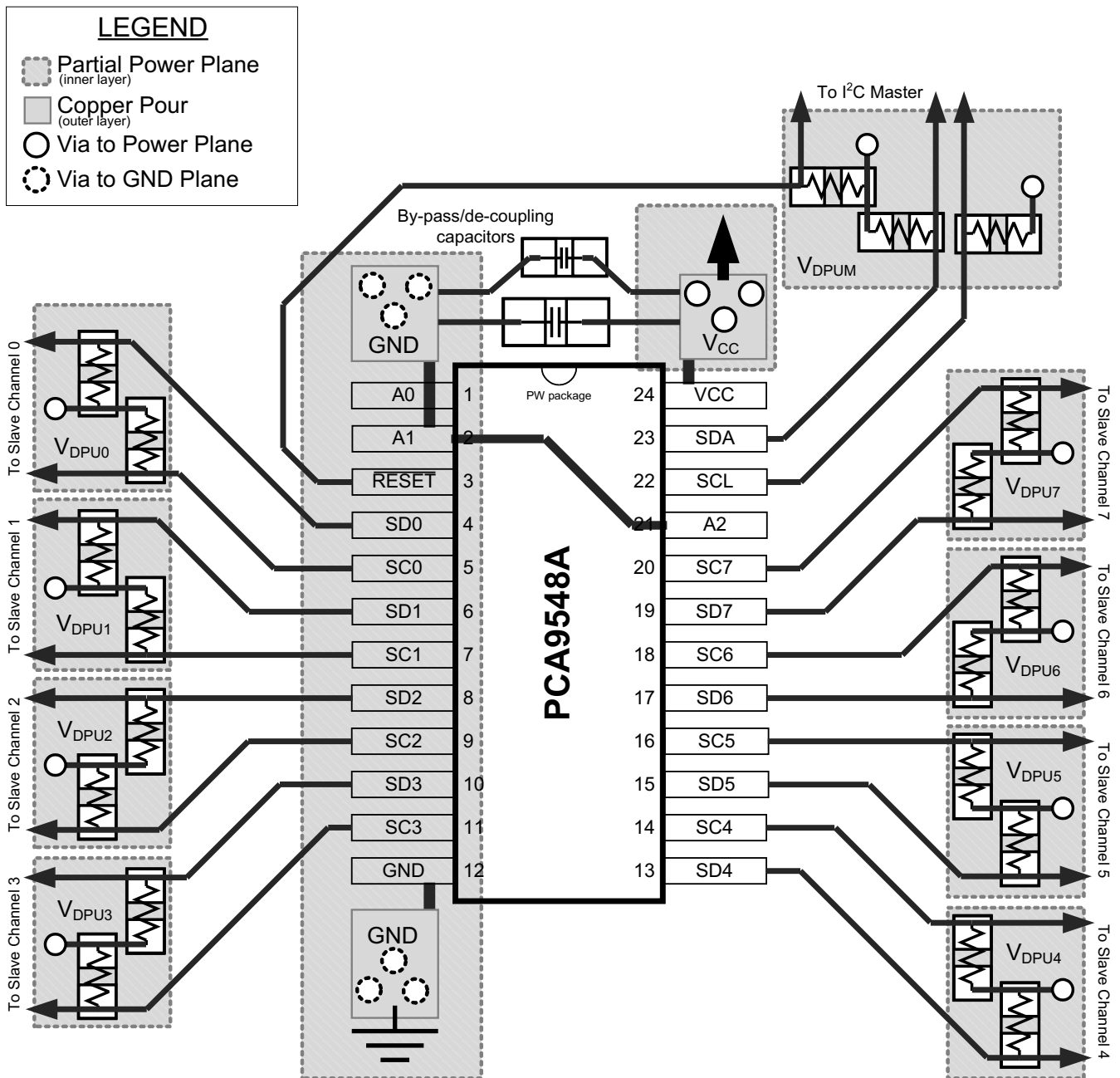


图 11-1. Layout Example

## 12 Device and Documentation Support

### 12.1 Related Documentation

For related documentation see the following:

- [I2C Bus Pull-Up Resistor Calculation](#)
- [Maximum Clock Frequency of I2C Bus Using Repeaters](#)
- [Introduction to Logic](#)
- [Understanding the I2C Bus](#)
- [Choosing the Correct I2C Device for New Designs](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](#). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Trademarks

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### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">PCA9548ADB</a>	Active	Production	SSOP (DB)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548ADB.A	Active	Production	SSOP (DB)   24	60   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
<a href="#">PCA9548ADBR</a>	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548ADBR.A	Active	Production	SSOP (DB)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548ADGV	NRND	Production	TVSOP (DGV)   24	-	-	Call TI	Call TI	-40 to 85	
<a href="#">PCA9548ADGVR</a>	NRND	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548ADGVR.A	NRND	Production	TVSOP (DGV)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
<a href="#">PCA9548ADW</a>	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A
PCA9548ADW.A	NRND	Production	SOIC (DW)   24	25   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A
<a href="#">PCA9548ADWR</a>	NRND	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A
PCA9548ADWR.A	NRND	Production	SOIC (DW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9548A
<a href="#">PCA9548APWR</a>	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548APWR.B	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548APWRG4	Active	Production	TSSOP (PW)   24	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD548A
PCA9548ARGER	NRND	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD548A
PCA9548ARGER.B	NRND	Production	VQFN (RGE)   24	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD548A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

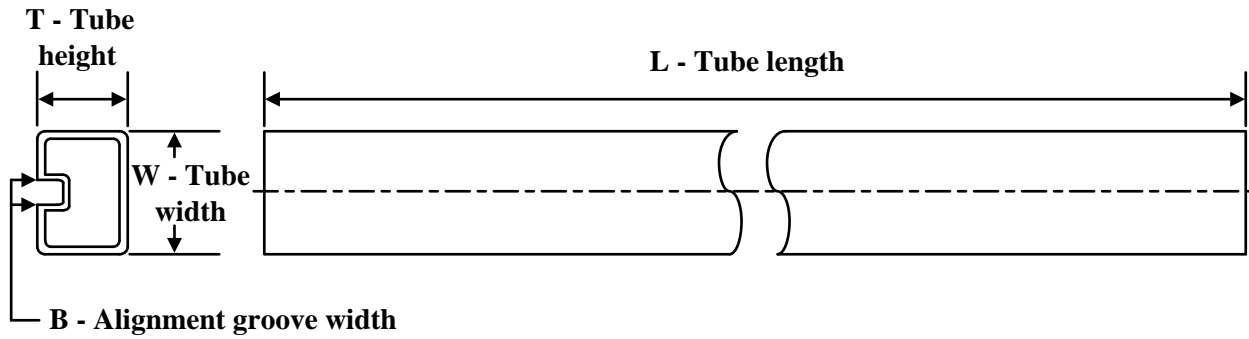

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9548ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCA9548ADGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9548ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCA9548ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

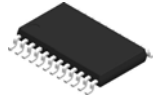
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9548ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
PCA9548ADGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
PCA9548ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCA9548ARGER	VQFN	RGE	24	3000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
PCA9548ADB	DB	SSOP	24	60	530	10.5	4000	4.1
PCA9548ADB.A	DB	SSOP	24	60	530	10.5	4000	4.1
PCA9548ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
PCA9548ADW.A	DW	SOIC	24	25	506.98	12.7	4826	6.6

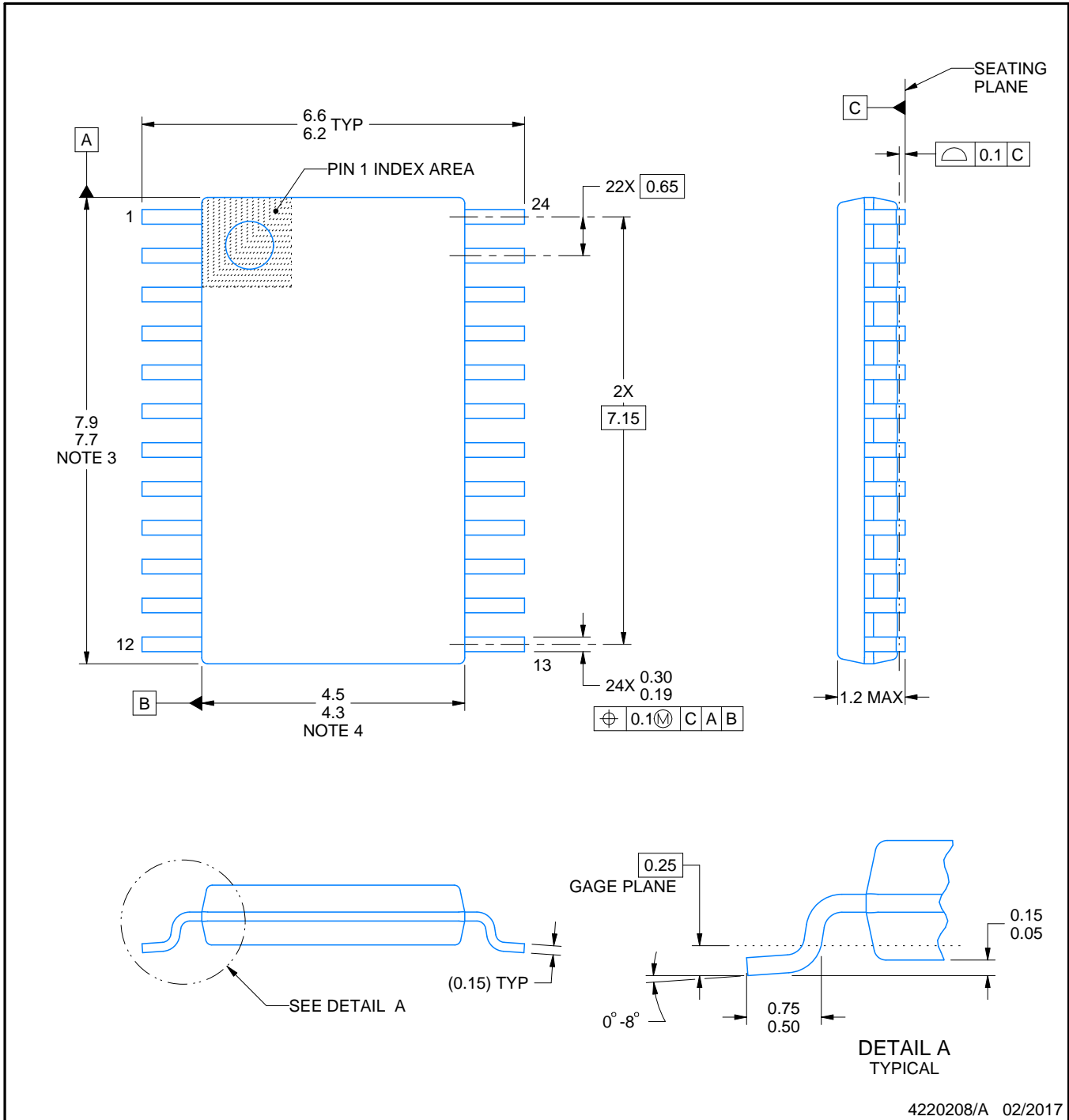
PW0024A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220208/A 02/2017

NOTES:

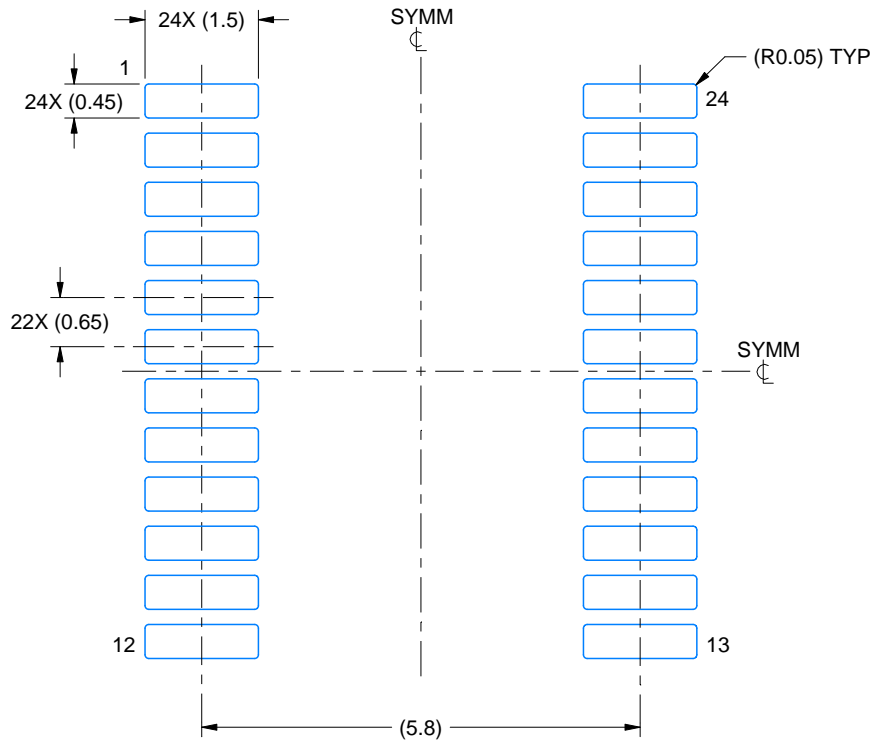
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

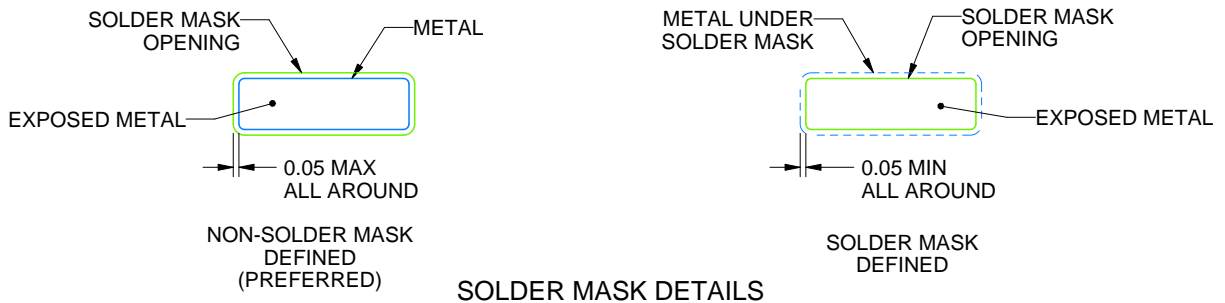
PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

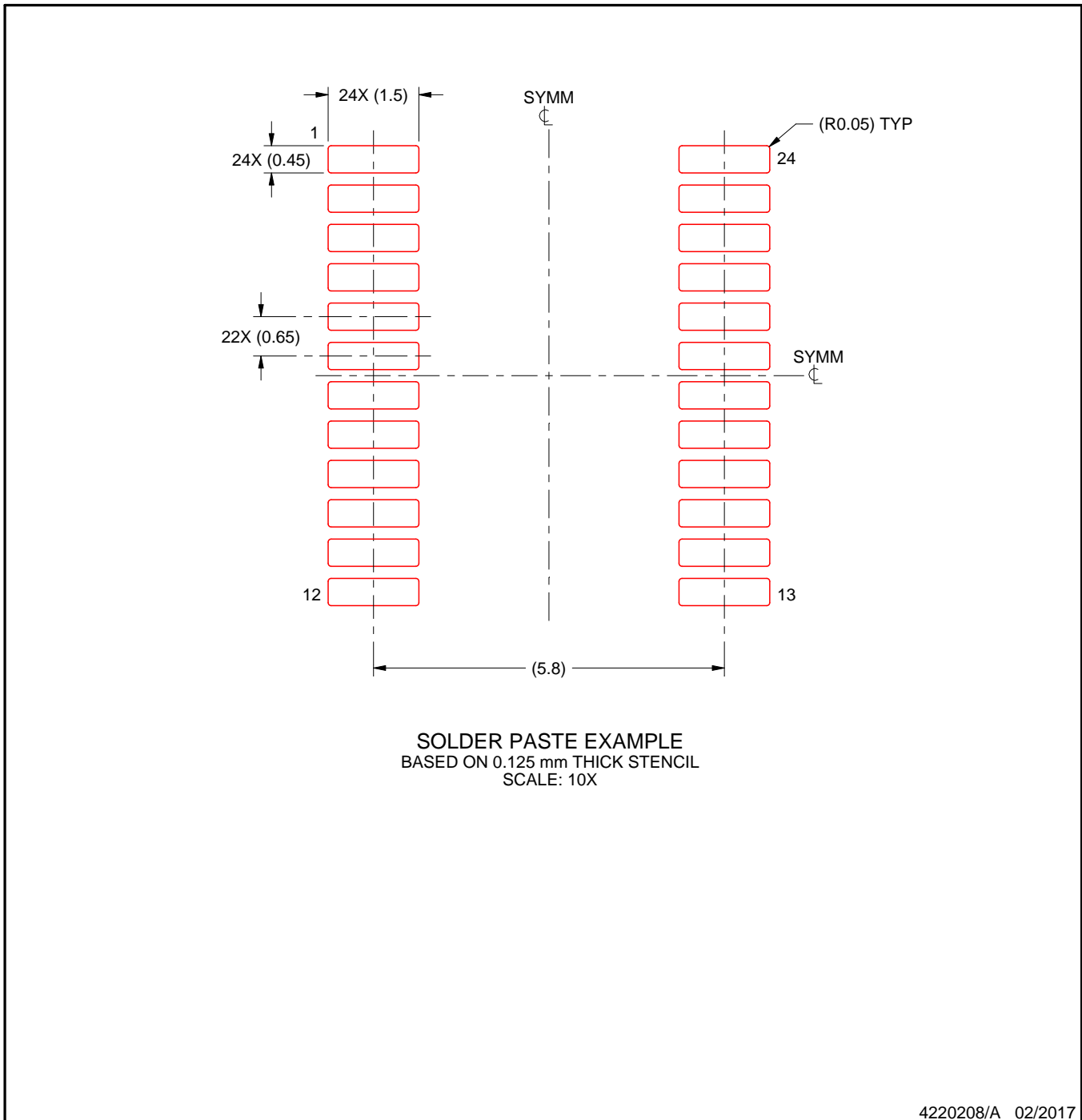
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

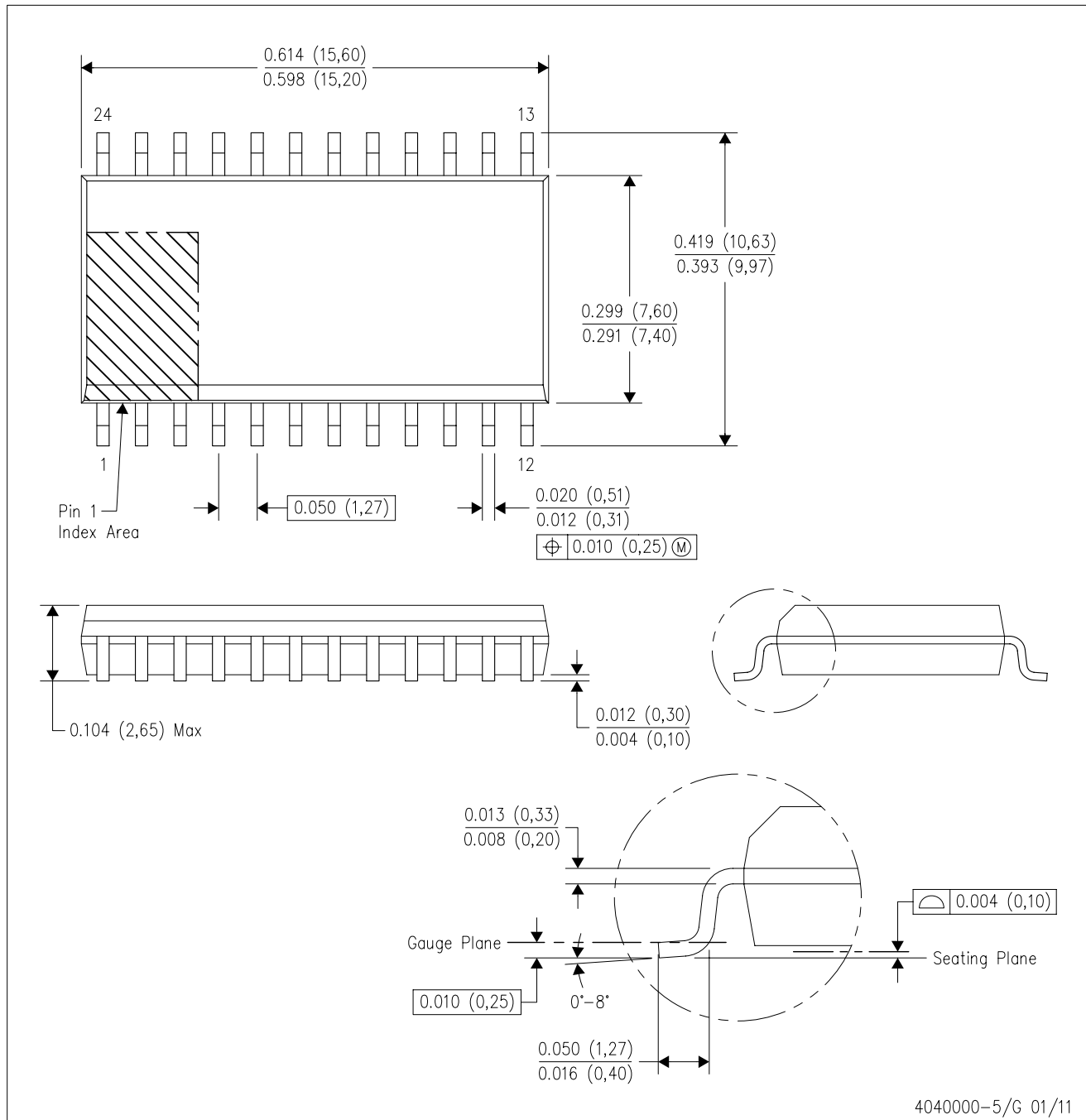


NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

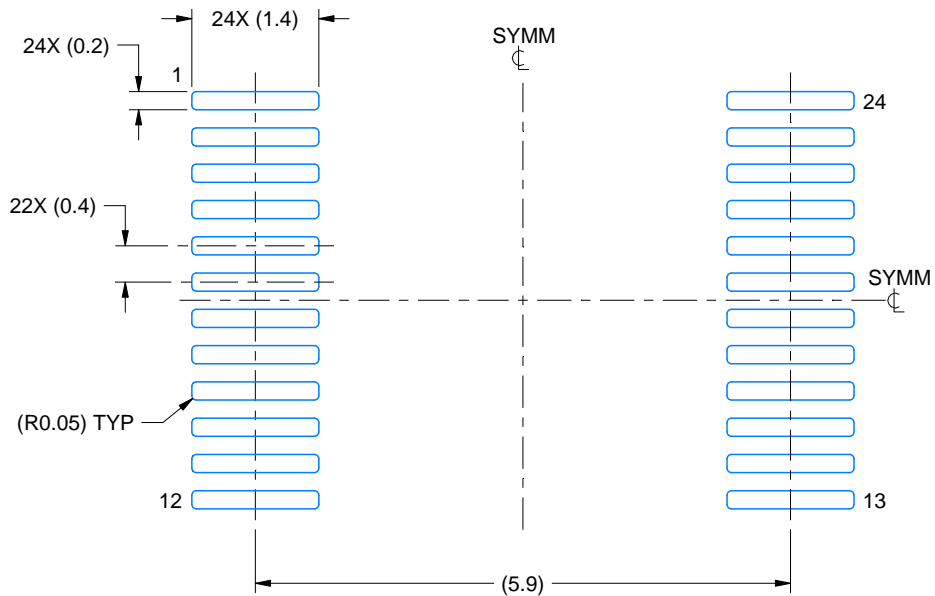


# EXAMPLE BOARD LAYOUT

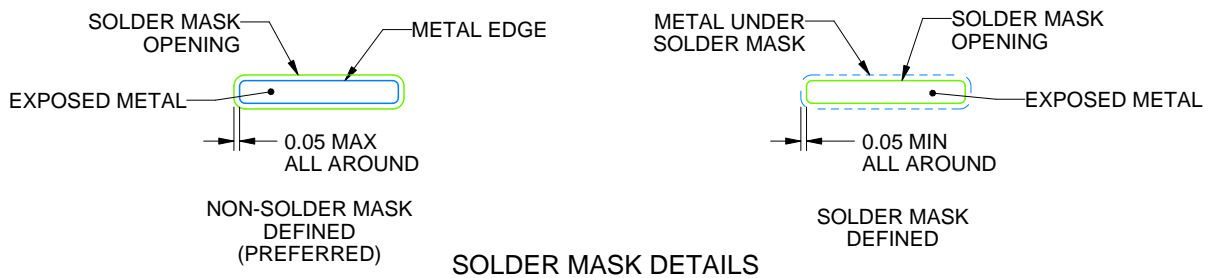
DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 12X



SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

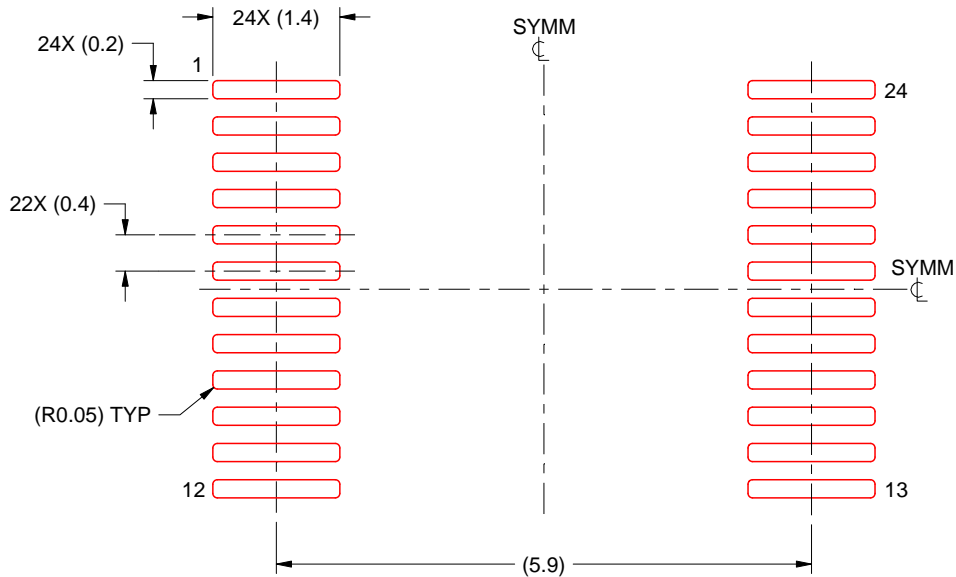
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGV0024A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 12X

4229221/A 12/2022

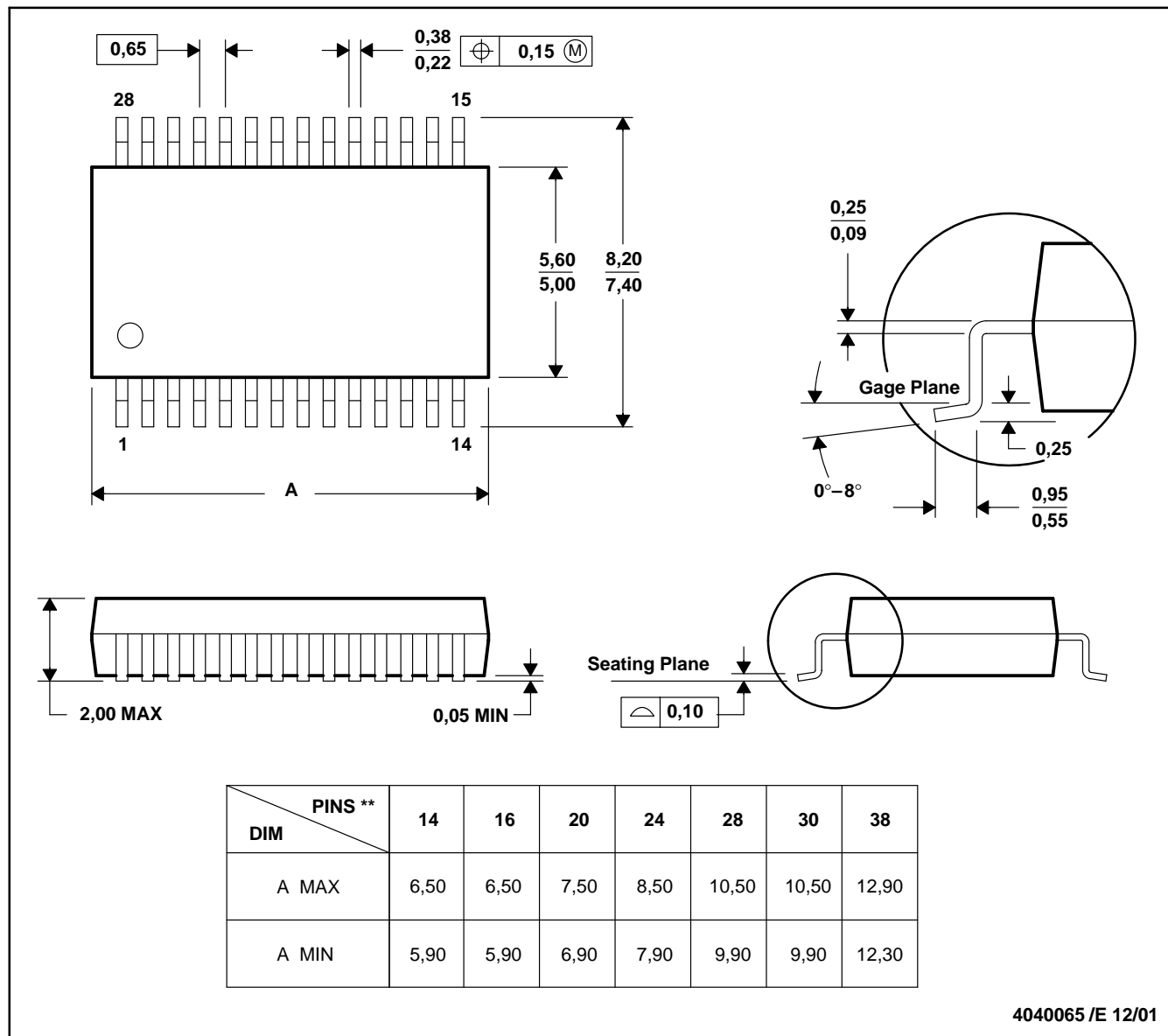
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



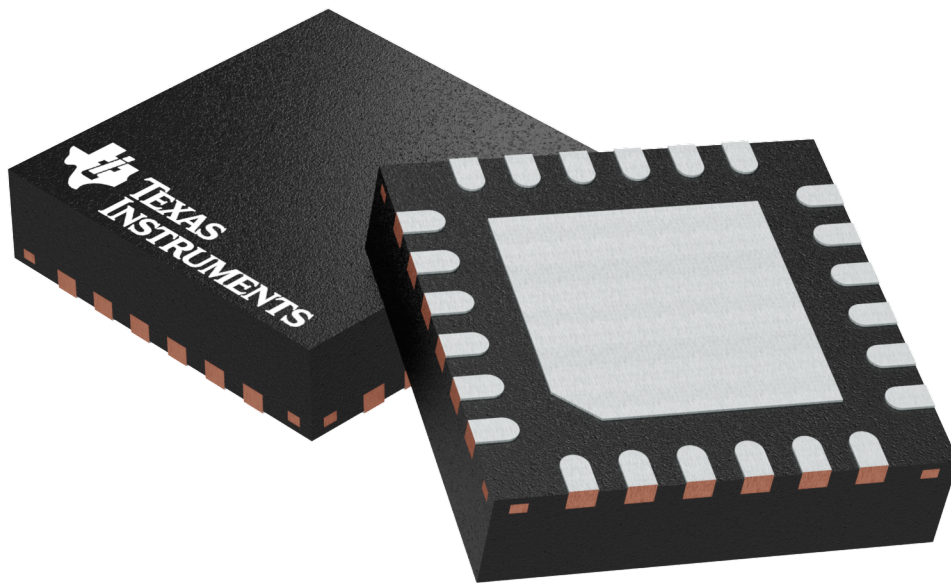
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

**RGE 24**

**GENERIC PACKAGE VIEW**

**VQFN - 1 mm max height**

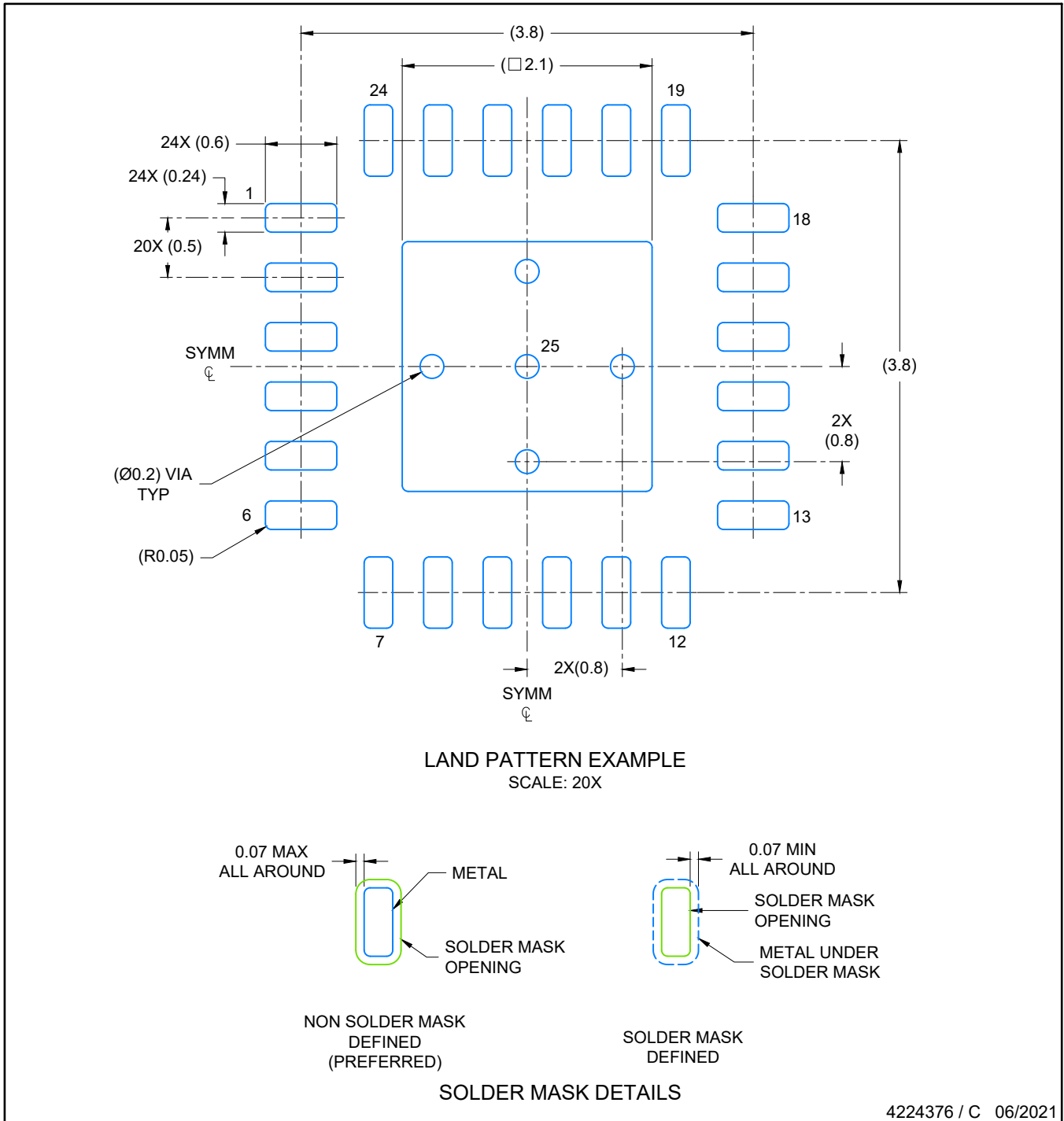
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H





4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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